

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-022684

(43)Date of publication of application : 22.01.2004

(51)Int.Cl.

H01L 33/00

H01L 21/205

(21)Application number : 2002-173503

(71)Applicant : SHOWA DENKO KK

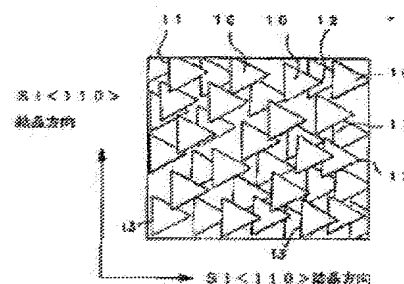
(22)Date of filing : 14.06.2002

(72)Inventor : UDAGAWA TAKASHI

(54) BORON PHOSPHIDE-BASED SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD, AND LIGHT EMITTING DIODE**(57)Abstract:**

PROBLEM TO BE SOLVED: To provide a boron phosphide-based semiconductor device which includes a boron phosphide semiconductor layer having a superior surface flatness and few crystal defects and which exhibits superior properties, and also to provide a method of manufacturing the same.

SOLUTION: The boron phosphide-based semiconductor device comprises a substrate made of single crystal silicon (Si) with {111} planes and the boron phosphide (BP) semiconductor layer formed on a front surface of the substrate. A lower part of the boron phosphide semiconductor layer is made of an amorphous material including boron (B) and phosphorus (P), while an upper part of it comprises a single crystal layer wherein a plurality of plate-like crystals, each being made of single crystal boron phosphide with {111} planes ({111}-single crystal boron phosphide) and having a nearly equilateral triangular planar shape, are connected to one after another.



* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.*** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]

A substrate which consists of a silicon (Si) single crystal which makes the surface a {111}-crystal face.

The Lynn-ized boron (BP) semiconductor layer provided on this substrate face.

It consists of a single crystal layer with which two or more plate crystals which are the Lynn-ized boron system semiconductor devices provided with the above, and make plane shape an approximately equilateral triangle were made to connect.

[Claim 2]

The Lynn-ized boron system semiconductor device according to claim 1, wherein each triangle of said plate crystal turns one vertex to a uniform direction and is arranged.

[Claim 3]

The Lynn-ized boron system semiconductor device according to claim 1 or 2, wherein one side of each triangle of said plate crystal is almost parallel to the <110> directions of a silicon single crystal board or is an abbreviated perpendicular.

[Claim 4]

On a substrate which consists of a silicon (Si) single crystal which makes the surface a {111}-crystal face, the Lynn-ized boron (BP) semiconductor layer which consists of a lower layer part and the upper levels in a manufacturing method of the Lynn-ized boron system semiconductor device to form A source of boron, The 1st process of supplying phosphorus sources of the 1st rate of the ratio of concentration (R_1) to concentration of a source of boron, and forming an amorphous lower layer part, Then, a rate of the ratio of concentration of phosphorus sources to a source of boron is made to increase to the 2nd bigger rate of the ratio of concentration (R_2) than R_1 temporally, By the 2nd process of forming the upper levels who consist of a single crystal layer with which two or more plate crystals which are the Lynn-ized boron single crystals ({111}-Lynn-ized boron single crystal) which make the surface a {111}-crystal face, and make plane shape an approximately equilateral triangle were made connecting on a lower layer part. A manufacturing method of the Lynn-ized boron system semiconductor device forming the Lynn-ized boron semiconductor layer.

[Claim 5]

A manufacturing method of the Lynn-ized boron system semiconductor device according to claim 4 making R_1 or less [0.2 or more] into 50, and making R_2 or less [500 or more] into 2000.

[Claim 6]

LED which is the Lynn-ized boron system semiconductor device given in any 1 paragraph of Claims 1-3, and provided and produced a luminous layer which consists of a gallium nitride indium mix crystal ($Ga_xIn_{1-x}N$) layer on the Lynn-ized boron semiconductor layer.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

With respect to the Lynn-ized boron system semiconductor device possessing the Lynn-ized boron semiconductor layer formed on the surface of a silicon (Si) monocrystal substrate, and its manufacturing method, this invention is excellent in especially surface surface smoothness, and relates to the Lynn-ized boron system semiconductor device possessing the Lynn-ized boron semiconductor layer with few crystal defects.

[0002]

[Description of the Prior Art]

Conventionally, since various semiconductor devices are constituted, the Lynn-ized boron (BP) semiconductor layer is used. For example, it is used for constituting the n form base (base) layer of a npn assembling-die hetero-bipolar transistor (HBT) (J. refer to Electrochem.Soc., 125 (4) and (1978), 633 - 637 pages). It is in a blue laser diode (LD), and is used as a contact (contact) layer for forming the low ohmic (Ohmic) electrode of contact resistance (refer to JP,H10-242567,A). It is used as a buffer layer for constituting the light emitting diode (LED) which brings about luminescence of short wavelength, such as blue glow (refer to U.S. Pat. No. 6,069,021 item).

[0003]

the halogen (halogen) method ("a Japanese crystal growth academic journal") the Lynn-ized boron semiconductor layer uses boron trichloride (BCl_3) and a phosphorus trichloride (PCl_3) as a starting material from the former Refer to Vol.24, and No. 2 (1997) or 150 pages, the hydride (hydride) method (J. — Crystal Growth — 24/25 (1974)) which uses borane (BH_3) or diborane (B_2H_6), phosphine (PH_3), etc. as a raw material refer to the 193-196 page and a molecular beam epitaxy (J. — Solid StateChem. and 133 (1997).) refer to the 269-272 page and the organometal chemistry gaseous phase depositing (MOCVD) method (Inst.Phys.Conf.Ser., No.129 (IOP Publishing Ltd. (UK, 1993).)) which uses an organic boron compound and the hydride of Lynn as a raw material It is formed by refer to the 157-162 page etc.

[0004]

The silicon single crystal (silicon) is chiefly used for the substrate to which vapor phase epitaxy of the Lynn-ized boron semiconductor layer is carried out [want / to make it] (above 1). J. Electrochem.Soc., 125 (1978) references. However, the grating constant of a silicon single crystal is 5.431Å, and the grating constant of cubic sphalerite type Lynn-ized boron is 4.538Å (refer to the Teramoto ****, "semiconductor device introduction" (March 30, 1995, Baifukan Issue First edition), and 28 pages). Therefore, the degree of lattice mismatch of a silicon single crystal and the Lynn-ized boron crystal is large with about 16.5% (refer to Katsufusa Shono work, "semiconductor technology (above)" (June 25, 1992, University of Tokyo Press issue 9 **), 97 - 98 pages).

[0005]

That the Lynn-ized boron semiconductor layer of a single crystal grows on a silicon single crystal board, For example, in halogen vapor phase growth, being limited to the range of 1020 to 1070 ** very narrow temperature [50 **] is found (the Nishinaga **, "applied physics" (refer to volume [45th] No. 9 (1976) and 891-897 pages)). By the hydride method used as a raw material, borane (BH_3) and phosphine (PH_3). It is based on a slight change of vapor-phase-epitaxy conditions, and being generated in the Lynn-ized boron semiconductor layer by the twin crystal (twinning) which is a kind of stacking fault (stacking fault) is taught (refer to the above-mentioned "the semiconductor technology (above)", 99 - 100 pages).

[0006]

[Problem(s) to be Solved by the Invention]

The problem of the conventional technology for carrying out the vapor-phase-epitaxy means of the Lynn-ized boron semiconductor layer on the silicon base surface, The lattice mismatch of the Lynn-ized boron semiconductor layer and a silicon single crystal was size, and since crystal composition or a manufacturing method effective in making it fully ease was not clear, it suited that the Lynn-ized boron semiconductor layer which is excellent in surface surface smoothness could not be obtained regularly. For the Reason of being generated by twin crystal therefore, it was primarily stabilized in change of the vapor-phase-epitaxy conditions few [range / the range of the temperature which can carry out vapor phase epitaxy of the Lynn-ized boron semiconductor layer of a single crystal is narrow, and], and the single crystal layer of Lynn-ized boron with few crystal defects was not able to be manufactured to it. Therefore, it is fully stabilized and did not come to provide the Lynn-ized boron system semiconductor device which can demonstrate the good characteristic.

[0007]

This invention is excellent in surface surface smoothness, and possesses the Lynn-ized boron semiconductor layer with

few crystal defects, and an object of this invention is to provide the Lynn-ized boron system semiconductor device which can demonstrate the good characteristic, and its manufacturing method.

[0008]

[Means for Solving the Problem]

Namely, this invention,

(1) A substrate which consists of a silicon (Si) single crystal which makes the surface a {111}-crystal face, In the Lynn-ized boron system semiconductor device provided with the Lynn-ized boron (BP) semiconductor layer provided on this substrate face, A lower layer part of this Lynn-ized boron semiconductor layer consists of an amorphous substance containing boron (B) and Lynn (P), The Lynn-ized boron system semiconductor device which the upper levels of this Lynn-ized boron semiconductor layer are the Lynn-ized boron single crystal ({111}-Lynn-ized boron single crystal) which makes the surface a {111}-crystal face, and is characterized by consisting of a single crystal layer with which two or more plate crystals which make plane shape an approximately equilateral triangle were made to connect.

(2) The Lynn-ized boron system semiconductor device given in the above (1), wherein each triangle of said plate crystal turns one vertex to a uniform direction and is arranged.

(3) one side of each triangle of said plate crystal is almost parallel to the <110> directions of a silicon single crystal board -- or -- abbreviated -- the Lynn-ized boron system semiconductor device the above (1) characterized by a vertical thing, or given in (2).

On a substrate which consists of a silicon (Si) single crystal which makes the surface a {111}-crystal face, the Lynn-ized boron (BP) semiconductor layer which consists of a lower layer part and the upper levels in a manufacturing method of the Lynn-ized boron system semiconductor device to form (4) A source of boron, The 1st process of supplying phosphorus sources of the 1st rate of the ratio of concentration (R_1) to concentration of a source of boron, and forming an amorphous lower layer part, Then, a rate of the ratio of concentration of phosphorus sources to a source of boron is made to increase to the 2nd bigger rate of the ratio of concentration (R_2) than R_1 temporally, By the 2nd process of forming the upper levels who consist of a single crystal layer with which two or more plate crystals which are the Lynn-ized boron single crystals ({111}-Lynn-ized boron single crystal) which make the surface a {111}-crystal face, and make plane shape an approximately equilateral triangle were made connecting on a lower layer part. A manufacturing method of the Lynn-ized boron system semiconductor device forming the Lynn-ized boron semiconductor layer.

(5) A manufacturing method of the Lynn-ized boron system semiconductor device given in the above (4) making R_1 or less [0.2 or more] into 50, and making R_2 or less [500 or more] into 2000.

(6) LED which is the Lynn-ized boron system semiconductor device the above (1) thru/or given in any 1 paragraph of (3), and provided and produced a luminous layer which consists of a gallium nitride indium mix crystal ($Ga_xIn_{1-x}N$) layer on the Lynn-ized boron semiconductor layer.

It comes out.

[0009]

[Embodiment of the Invention]

The Lynn-ized boron semiconductor layer concerning this invention depends on vapor-phase-epitaxy means, such as the halogen process, the hydride method, a molecular beam epitaxy, and the MOCVD method, and is grown up on the surface of the silicon single crystal ({111}-silicon single crystal) which makes the surface a {111}-crystal face. Since Si atom exists in the {111}-crystal face which makes the surface of a {111}-silicon single crystal densely as compared with other mirror (Miller) index sides of the low next, it is controlling osmosis in boron and the inside of a silicon single crystal board of Lynn, and diffusion with dominance. As a temperature which carries out vapor phase epitaxy, 750 ** - 1200 ** are suitable. Since it is generated by the Lynn-ized boron crystal (J. refer to Am.Ceramic Soc., 47 (1) and (1964), 44 - 46 pages) of polymers, such as $B_{13}P_2$, the elevated temperature over 1200 ** becomes inconvenient for forming the Lynn-ized boron layer of the single crystal of a monomer. In order not to make the oxidized silicon film which blocks growth of the Lynn-ized boron semiconductor layer form in the surface, it is preferred for a silicon single crystal board to heat not within oxygen environment but in the atmosphere of a non-oxidizing quality. In order to avoid formation of the silicon nitride film which blocks the vapor phase epitaxy of the Lynn-ized boron semiconductor layer (masking), heating in the atmosphere which does not contain nitrogen (N_2) is suitable. The atmosphere which consists of monatomic inactive gas, such as a hydrogen atmosphere or argon (Ar), can be used suitably.

[0010]

The Lynn-ized boron semiconductor layer of this invention has the feature in internal crystal composition, and the lower layer part comprises an amorphous substance including boron and Lynn. A lower layer part is a layer located in a downward pars basilaris ossis occipitalis to the surface of the Lynn-ized boron semiconductor layer. An amorphous layer including boron and Lynn can be formed by making the ratio of the concentration of the phosphorus sources to the concentration of the source of boron at the time of vapor phase epitaxy, and what is called a V/III ratio into a low value in comparison. It can form efficiently by setting a V/III ratio or less to 50 by 0.2 or more especially. The concentration of the source of boron and phosphorus sources shall be expressed with molar concentration, respectively. In less than 0.2 extremely low V/III ratio, the concentration of boron becomes superfluous relatively and the inconvenience concluded in the amorphism layer which lacks in the surface smoothness of the surface where the crystal grain of hemispherical boron crowded is produced. In the V/III ratio exceeding 50, the Lynn-ized boron layer of the polycrystal with which single crystal grains are scattered may be formed in an amorphous layer, an amorphous substance cannot be formed certainly, and it is not desirable. It can be amorphous, or distinction of polycrystal and a single crystal depends on an X diffraction means or an electron diffraction method, and it can distinguish.

[0011]

On the amorphous layer to which vapor phase epitaxy of the V/III ratio was carried out as the 1st above-mentioned V/III ratio (it is considered as R_1), the single crystal layer of Linn-ized boron is formed with the 2nd V/III ratio (it is considered as R_2) as the upper levels of the Linn-ized boron semiconductor layer. The upper levels of the Linn-ized boron semiconductor layer of this invention are the Linn-ized boron single crystal ([111]-Linn-ized boron single crystal) which makes the surface a {111}-crystal face, and consist of a single crystal layer which two or more plate crystals 10 which have the plane shape of an approximately equilateral triangle accumulated so that it may illustrate typically to drawing 1. A length of one side of the plate crystal 10 is about 100–200 nm here. It is the feature that the plate crystal 10 is arranged in the direction with the same vertex 12 to the triangular base 11. By arranging the plate crystal 10 uniformly in the same direction, have arranged in the position of mirror image relationship. Generating of the twin crystal resulting from the so-called crystalline (refer to Ryukichi Hashiguchi, **** *, a "thin film surface phenomenon" (Asakura Publishing issue material science lecture 6), 49 – 50 pages) of double arrangement (double spacing) can be prevented, and effect can be achieved for obtaining the Linn-ized boron single crystal layer with few crystal defects. The direction by which the tabular single crystal body of the approximately equilateral triangle is arranged depends on observation of the surface of the Linn-ized boron single crystal layer which used the atomic force microscope (AFM), for example, and can be judged.

[0012]

Especially, if 13 [one-side] is arranged so that it may become almost parallel to the $\langle 110 \rangle$ crystal orientation of a silicon single crystal, the plate crystal 10 of an approximately equilateral triangle, it is that cleavage divides the Linn-ized boron single crystal layer simply conjointly with the cleavage directions of the silicon single crystal of a diamond) crystal structure being $\langle 110 \rangle$ crystal orientation with convenience. 13 [one-side] is made almost parallel to the $\langle 110 \rangle$ crystal orientation of a silicon single crystal board, or vertical, and in order to carry out vapor phase epitaxy of the plate crystal of the Linn-ized boron arranged uniformly in the same direction, it is necessary to make the 2nd ratio ($=R_2$) or less into 2000 by 500 or more. It is so preferred to make R_2 into a high price that temperature to which vapor phase epitaxy of the plate crystal is carried out is made into an elevated temperature. The 2nd ratio ($=R_2$) depends on mass flowmeter (MFC) etc., and the amount of supply of the source of boron at the time of vapor phase epitaxy and phosphorus sources is controlled precisely, and it adjusts it. [as well as the 1st ratio ($=R_1$)] The thickness of the tabular Linn-ized boron single crystal body is controllable if the feed time of the source of boron is adjusted.

[0013]

The tabular Linn-ized boron single crystal body of the approximately equilateral triangle roundish to the top part in the 2nd ratio ($=R_2$) being less than 500 is obtained, and, as for many, the layer in which these plate crystals and amorphous substances are intermingled is obtained. If R_2 exceeds 2000, the tabular Linn-ized boron single crystal body of the approximately regular triangle form which has one side almost parallel to the {110} crystal orientation of a silicon single crystal board or vertical may not come to be stabilized. The angle which the {110} crystal orientation of a silicon single crystal and one side of the tabular single crystal body of approximately regular triangle form make tends to become large, so that R_2 is made large. If thickness of an amorphous layer which, in addition, carries out vapor phase epitaxy of the R_2 with the ratio of R_1 for setting it as the above-mentioned suitable ratio is made thin, The tabular Linn-ized boron single crystal body of the approximately equilateral triangle which arranges in the uniform direction and makes one side almost parallel to the {110} crystal orientation of a silicon single crystal board or vertical can be obtained. The thickness of an amorphous layer may be 20 nm or less at not less than 2 nm preferably. Amorphous thickness increases, and the influence of the {111}-crystal face of a silicon single crystal becomes weaker, and even the tabular Linn-ized boron single crystal body which makes plane shape an approximately triangle is no longer obtained regularly.

[0014]

A V/III ratio can be increased if the quantity of the amount of supply of phosphorus sources is made to increase gradually temporally in order to make a V/III ratio increase from R_1 to R_2 for example, holding uniformly the amount of supply to a vapor-phase-epitaxy system of the source of boron. For example, setting the amount of supply of $_3(C_2H_5) B$ constant, the flow of PH_3 is made to increase gradually and a V/III ratio is made to increase. Or maintaining the amount of supply of phosphorus sources uniformly, the amount of supply of the source of boron is decreased, and a V/III ratio is made to increase to R_2 . Or the amount of supply of phosphorus sources is made to increase by the rate of increase which exceeds the rate of increase of the amount of supply of the source of boron, and a V/III ratio is made to increase. It is preferred for the source of boron to supply so that the growth rate (increasing speed of thickness) of the tabular Linn-ized boron single crystal body of an approximately equilateral triangle may be set to per minute 15 to 30 nm/m. Decreasing a growth rate extremely causes extension of growth time. That is, the inconvenience which makes the time when an amorphous layer including a silicon single crystal board and boron, and Linn is exposed at an elevated temperature extend, promotes the reaction of boron or Linn, and Si crystal, and makes the joining interface of a silicon single crystal board and an amorphous layer make it disorderly is caused.

[0015]

The upper levels' Linn-ized boron single crystal layer is constituted from the tabular {111}-Linn-ized boron single crystal body like the above by the approximately regular triangle form arranged with a fixed direction. Therefore, it is the good Linn-ized boron single crystal with little twin crystal (or stacking fault) contained. Since the surface of each tabular single crystal body comprises uniformly a {111}-crystal face of the Linn-ized boron arranged in parallel with the {111}-silicon crystal face which makes the surface of a {111}-silicon single crystal board, it is flat. Therefore, on the

Lynn-ized boron single crystal layer concerning this invention, there is also little twin crystal to spread and the upper layer which is excellent in surface smoothness can be formed. For example, a good crystalline gallium nitride (GaN) system semiconductor layer with small crystal defect density can be formed as the upper layer. The Lynn-ized boron system semiconductor device, for example, LED, provides and constitutes the input output electrode of ohmic (Ohmic) nature in the laminated structure body provided with the GaN layer which is excellent in the above-mentioned crystallinity as a lower clad layer.

[0016]

[Function]

. Include the boron and Lynn which were formed with 1st V/III ratio R_1 , and also [amorphous] carried out vapor phase epitaxy. Making plane shape into an approximately equilateral triangle, the plate-like single crystal body which consists of a {111}-Lynn-ized boron single crystal uniformly arranged in the same direction has the operation which brings about the Lynn-ized boron semiconductor layer containing a good single crystal layer with low twin crystal (or stacking fault) density. almost parallel to the <110> crystal orientation of the silicon single crystal board which is especially a cleavage direction -- or -- abbreviated -- the tabular single crystal body which consists of a {111}-Lynn-ized boron single crystal which arranged one side of an approximately equilateral triangle in the vertical direction has the operation which makes easy cleavage to the <110> crystal orientation of the Lynn-ized boron semiconductor layer.

[0017]

[Example]

(The 1st working example)

In the 1st working example, the case where depended on the ordinary pressure MOCVD means and vapor phase epitaxy of the Lynn-ized boron (BP) semiconductor layer is carried out on a (111)-silicon single crystal board is made into an example, and the contents of this invention are explained concretely.

[0018]

In the 1st working example, the silicon single crystal which uses as the surface - (111) silicon crystal face which used the angle in [110] crystal orientation and inclined 2 degrees was used as a substrate. It inserted in the vapor-phase-epitaxy field in the product MOCVD vapor-phase-epitaxy furnace made from a quartz rectangular pipe of a high grade, after laying a substrate horizontally on the mounting base (susceptor) made from high grade graphite. Then, temperature up of the temperature of a substrate was carried out to 850 °C with the high-frequency-induction-heating method, circulating in a vapor-phase-epitaxy furnace considering about 16 l/m of high-purity-hydrogen gas as carrier (carrier) gas. The appropriate back supplied the phosphine (PH_3) made into the boron triethyl (C_2H_5) ($_3\text{B}$) made into the source of boron, and phosphorus sources to the vapor-phase-epitaxy field. Boron triethyl was supplied by making it foam with hydrogen gas and making the steam of boron triethyl accompany to the foaming service-water matter gas. The flow of foaming service-water matter gas was precisely controlled to 45 cc/m using electronic formula mass flowmeter (MFC). setting the concentration of the boron triethyl accompanied to a normal condition (0 °C, 1 atmosphere) -- per minute -- it was converted with the 1.34×10^{-4} mol (mol). On the other hand, concentration of the phosphine supplied to a vapor-phase-epitaxy field was considered as a part for 2.14×10^{-3} /. That is, the V/III ratio was set to 16.0. The circulation to the vapor-phase-epitaxy field of the source of boron and phosphorus sources was continued [while supplying the source of boron, and phosphorus sources by the above-mentioned concentration, and] for 2.5 minutes, maintaining a V/III ratio into the 1st above-mentioned ratio (R_1 , however $R_1=16$). From this, the amorphous layer including the boron which sets thickness to 20 nm, and Lynn was formed on the (111)-Si substrate.

[0019]

The concentration of the source of boron supplied to a vapor-phase-epitaxy field was reduced and combined with a part for 1.49×10^{-5} mol/, and the amount of supply of phosphorus sources was made to increase to a part for 1.93×10^{-2} mol/at the same time it terminated the vapor phase epitaxy of the above-mentioned amorphous layer. That is, the V/III ratio was raised from the 1st V/III ratio (R_1) to 1295.3 of the 2nd V/III ratio (R_2). Maintaining the 2nd V/III ratio to this value, supply of the source of boron and phosphorus sources was continued for 5 minutes, and the Lynn-ized boron semiconductor layer of p form which sets thickness to 300 nm was formed on the above-mentioned amorphous layer. After suspending supply to the vapor-phase-epitaxy field of the source of boron and ending formation of the Lynn-ized boron semiconductor layer, the (111)-silicon single crystal board was cooled compulsorily to the temperature near the room temperature, and automatically within the gaseous mixture atmosphere which consists of hydrogen carrier gas and phosphine.

[0020]

After cooling, it depended on general X diffraction measurement and electron diffraction measurement, and the crystalline form of the above-mentioned amorphism layer was checked. the halo which does not have a diffraction mottle in X diffraction measurement and electron diffraction measurement -- the (halo) diffraction pattern was obtained and having been an amorphous layer was admitted. On the other hand, the diffraction from the (111)-crystal face of Lynn-ized boron appeared in the X diffraction pattern of the Lynn-ized boron semiconductor layer. The appearance of the clear diffraction peak from the (111)-crystal face of the Lynn-ized boron semiconductor layer wrote the amorphous layer with the thin layer moderate like the 1st working example, and since the arrangement of -Si crystal face which makes the surface of a substrate (111) was inherited, it was interpreted. When the surface of the Lynn-ized boron semiconductor layer was observed using the common atomic force microscope (AFM), it was recognized visually that two or more plate crystals of an approximately equilateral triangle which was illustrated to drawing 1 are accumulating all over the surface reflecting

the plane shape of a (111)-Lynn-ized boron crystal. The plate crystal of the approximately equilateral triangle had aligned in the uniform direction parallel to the $\langle 110 \rangle$ directions of the silicon single crystal of a substrate.

[0021]

(The 2nd working example)

In the 2nd working example, the case where LED is produced using the laminated structure body provided with the Lynn-ized boron semiconductor layer concerning this invention is made into an example, and the contents of this invention are explained concretely.

[0022]

The mimetic diagram of LED1A concerning the 2nd working example is shown in drawing 2. The cross section of LED1A in alignment with dashed line X-X' shown in drawing 2 is shown in drawing 3.

[0023]

By the same method as the 1st above-mentioned working example, on the p (111)-silicon single crystal board 101 of type, Vapor phase epitaxy of the amorphous layer 102 which includes boron and Lynn by making a V/III ratio into R_1 ($=16.0$) was carried out, and vapor phase epitaxy of the p form Lynn-ized boron semiconductor layer 103 was further carried out by making a V/III ratio into R_2 ($=1295.3$). In LED concerning the 2nd working example, p form Lynn-ized boron semiconductor layer 103 which consists of a (111)-Lynn-ized boron single crystal of a monomer was used as the lower clad layer 103. the carrier concentration of -p type Lynn-ized boron semiconductor layer which makes the lower clad

layer 103 (111) — about — it was $2 \times 10^{19} \text{ cm}^{-3}$.

[0024]

On the lower clad layer 103, the upper clad layer 105 which consists of the luminous layer 104 and an n form Lynn-ized boron layer was made to laminate one by one, and the laminated structure body 1B of the LED1A use was formed. The luminous layer 104 consisted of gallium nitride indium mix crystal ($\text{Ga}_x\text{In}_{1-x}\text{N}$) layers of n form. A $\text{Ga}_x\text{In}_{1-x}\text{N}$ layer, It formed at 850 ** using the MOCVD method of trimethylgallium (CH_3)₃Ga / trimethylindium (CH_3)₃In / ammonia (NH_3) / nitrogen (N_2) system of reaction. The indium composition ratio ($=1-x$) of $\text{Ga}_x\text{In}_{1-x}\text{N}$ of a hexagonal wurtzite crystal form, It could be 10% ($=0.10$) so that it might become a grating constant of the a-axis corresponding to the interval (about 3.21Å) of the [110]-crystal face of the Lynn-ized boron which crosses at right angles to the (111)-crystal face of the Lynn-ized boron which makes the surface of p form Lynn-ized boron semiconductor layer 103. Next, the addition to the foaming service-water matter gas and the vapor-phase-epitaxy field of phosphine which accompany the steam of boron triethyl was resumed, and the Lynn-ized boron crystal layer of n form which makes the upper clad layer 105 was formed. The thickness of n form Lynn-ized boron crystal layer 105 could be about 300 nm. The carrier concentration of the same layer 105 which depended on the usual electrolysis C-V method, and was measured was

abbreviation $1 \times 10^{19} \text{ cm}^{-3}$. The addition to the vapor-phase-epitaxy field of the foaming service-water matter gas which accompanies the steam of boron triethyl was stopped, and formation of n form Lynn-ized boron crystal layer 105 was ended. Then, the temperature of the laminated structure body 1A was lowered at about 600 ** in the mixed atmosphere of phosphorus sources (PH_3) and hydrogen carrier gas. Then, supply of PH_3 to a vapor-phase-epitaxy field was suspended, and the laminated structure body 1A was cooled to near the room temperature in H_2 air current.

[0025]

The n form ohmic electrode 107 which becomes a side in contact with the same layer 105 from the three-layer layered structure of Au-germanium / nickel (nickel) / Au which has arranged gold and a germanium (Au-germanium) alloy film was formed in the center section of the upper clad layer 105 which consists of an n form Lynn-ized boron crystal layer which makes the surface of the laminated structure body 1B. The n form ohmic electrode 107 which serves as the plinth (pad) electrode for connection was used as the circular electrode which shall be about 150 micrometers in diameter. To the approximately whole area of the rear face of p form silicon single crystal board 101, the p form ohmic electrode 108 which consists of gold (Au) has been arranged. The thickness of Au vacuum evaporation film could be about 3 micrometers. LED1A of the pn junction type DH structure which pinched the n form luminous layer 104 in p form Lynn-ized boron layer 103 and n form Lynn-ized boron layer 105 consisted of this. Since each had about 3-eV band gap at a room temperature, p form Lynn-ized boron layer 103 and n form Lynn-ized boron layer 105 have been effectively used as a barrier layer (clad) layer to the luminous layer 104.

[0026]

Cleavage of the laminated structure body 1B was carried out to the $\langle 110 \rangle$ crystal orientation of the silicon single crystal board 101, and it divided into the chip (chip) of the square which sets one side to about 350 micrometers. Since - plate crystal which makes the (111)-Lynn-ized boron semiconductor layer of the lower clad layer 103 (111) arranged one side uniformly in the direction parallel to the $\langle 110 \rangle$ directions, or vertical, cleavage to $\langle 110 \rangle$ crystal orientation has been carried out easily. When conduction of the actuating current of 20 mA (mA) was carried out to the forward direction between the n form ohmic electrode 107 and p form OMITSU electrode 108, the violet band light which shall be about 440 nm in wavelength from LED1A was emitted. The luminosity in the chip state measured using a common integrating sphere will be a 9-mcd (mcd), and LED1A of high luminescence intensity will be provided. Since the surface of p form Lynn-ized boron semiconductor layer 103 provided via the amorphous layer 102 including boron and Lynn was what is excellent in surface smoothness, it has formed the pn junction structure which makes a joining interface flat by the n form luminous layer 104. p form Lynn-ized boron semiconductor layer 103 with the flat surface was written with the foundation layer, and the surface of the luminous layer 104 also became flat conveniently, and has formed the pn junction structure of the flat joining interface by the upper clad layer 105. for this reason, forward voltage (however, when forward

current is 20 mA) -- about -- it will be referred to as 3.1V and Lynn-ized boron system LED which has a rectifying characteristic based on the good pn junction structure which makes reverse voltage more than 5V (however, when a reverse current is set to 10microA) will be provided.

[0027]

[Effect of the Invention]

In the Lynn-ized boron system semiconductor device provided with the substrate which consists of a silicon single crystal which makes the surface a {111}-crystal face, and the Lynn-ized boron semiconductor layer provided on the {111}-crystal face of a substrate face, if it depends on this invention, The lower layer part of this Lynn-ized boron semiconductor layer consists of an amorphous substance containing boron (B) and Lynn (P). The upper levels of this Lynn-ized boron semiconductor layer are the Lynn-ized boron single crystal ({111}-Lynn-ized boron single crystal) which makes the surface a {111}-crystal face. Since it constituted so that it might consist of a single crystal layer with which two or more plate crystals which make plane shape an approximately equilateral triangle were made to connect, there is nothing to the former and the vapor phase epitaxy of the Lynn-ized boron single crystal layer which is excellent in surface surface smoothness can be carried out in a wide temperature requirement. Therefore, if the pn junction structure which has a flat joining interface can be constituted and being spread, it can contribute for bringing about the Lynn-ized boron system semiconductor light emitting element with a good rectifying characteristic.

[0028]

Since each triangle of the plate crystal of the upper levels who make the Lynn-ized boron semiconductor layer turns one vertex to a uniform direction and was arranged in this invention again, Effect can be achieved for being stabilized and carrying out vapor phase epitaxy of the Lynn-ized boron single crystal layer which is excellent in crystallinity with small crystal defect densities, such as twin crystal, and if spread, it can contribute for bringing about the Lynn-ized boron system semiconductor device which can demonstrate the good pn junction characteristic.

[0029]

Since we decided to make it align in the uniform direction and to arrange in this invention so that one side of each triangle of the plate crystal which forms the upper levels of the Lynn-ized boron semiconductor layer might be almost parallel to the <110> directions of a silicon single crystal board or might be an abbreviated perpendicular, The simply individual Lynn-ized boron system semiconductor device is obtained using the cleavage to the <110> directions of a silicon single crystal.

[0030]

If it depends on this invention, after forming a lower layer part amorphous as 50 or less for the rate of the ratio of concentration of the source of boron, and phosphorus sources supplied at the time of vapor phase epitaxy or more by 0.2, By making the rate of the ratio of concentration of the source of boron, and phosphorus sources or less into 2000 by 500 or more [bigger], and carrying out vapor phase epitaxy of the plate crystal which consists of a {111}-Lynn-ized boron single crystal of an approximately equilateral triangle on amorphous, Since the Lynn-ized boron single crystal layer which makes the upper levels is formed, crystal defect densities, such as twin crystal, are low, it excels in surface surface smoothness, and effect is taken by bringing about the Lynn-ized boron single crystal layer which makes easy separation for the individual element which depends on cleavage.

[Brief Description of the Drawings]

[Drawing 1] It is a mimetic diagram showing the upper levels of the Lynn-ized boron semiconductor layer which consists of a single crystal layer with which two or more plate crystals which make plane shape an approximately equilateral triangle were made to connect.

[Drawing 2] It is a mimetic diagram of LED concerning the 1st working example of this invention.

[Drawing 3] It is a cross section in alignment with dashed line X-X' of LED shown in drawing 2.

[Description of Notations]

10 The plate crystal which consists of a Lynn-ized boron single crystal which makes plane shape an approximately equilateral triangle

11 The base of a plate crystal

12 The one peak of a plate crystal

13 One side of a plate crystal

1A LED

1B Laminated structure body

101 Monocrystal substrate

102 Amorphous layer

103 Lynn-ized boron single crystal layer (lower clad layer)

104 Luminous layer

105 Upper clad layer

107 n form ohmic electrode

108 p form ohmic electrode

[Translation done.]

(19) 日本国特許庁(JP)

(12) 公開特許公報(A)

(11) 特許出願公開番号

特開2004-22684

(P2004-22684A)

(43) 公開日 平成16年1月22日(2004.1.22)

(51) Int. Cl.⁷

H01L 33/00

H01L 21/205

F I

H01L 33/00

H01L 21/205

C

テーマコード(参考)

5F041

5F045

審査請求 未請求 請求項の数 6 O L (全 9 頁)

(21) 出願番号

特願2002-173503(P2002-173503)

(22) 出願日

平成14年6月14日(2002.6.14)

(71) 出願人 000002004

昭和電工株式会社

東京都港区芝大門1丁目13番9号

(74) 代理人 100118740

弁理士 柿沼 伸司

(72) 発明者 宇田川 隆

埼玉県秩父市大字下影森1505番地 昭

和電工株式会社研究開発センター内

Fターム(参考) 5F041 CA04 CA23 CA33 CA34 CA65

CA77 CA82 CA83 CA92

5F045 AA04 AB15 AB17 AC01 AC08

AC09 AC12 AC15 AD12 AE29

AF03 AF04 AF13 EE04

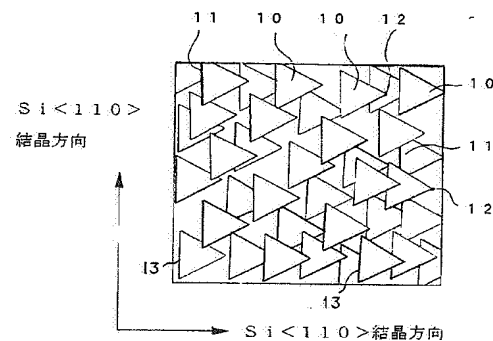
(54) 【発明の名称】 リン化硼素系半導体素子、その製造方法およびLED

(57) 【要約】

【課題】 表面の平坦性に優れ結晶欠陥が少ないリン化硼素半導体層を具備し、良好な特性を発揮できるリン化硼素系半導体素子とその製造方法を提供する。

【解決手段】 表面を{111}-結晶面とする珪素(Si)単結晶からなる基板と、該基板表面上に設けられたリン化硼素(BP)半導体層とを備えたリン化硼素系半導体素子に於いて、該リン化硼素半導体層の下層部が、硼素(B)とリン(P)とを含む非晶質からなり、該リン化硼素半導体層の上層部が、表面を{111}-結晶面とするリン化硼素単結晶({111}-リン化硼素単結晶)であって、平面形状を略正三角形とする複数の板状結晶を連結させた単結晶層からなる。

【選択図】 図1



【特許請求の範囲】

【請求項1】

表面を{111}-結晶面とする珪素(Si)単結晶からなる基板と、該基板表面上に設けられたリン化硼素(BP)半導体層とを備えたリン化硼素系半導体素子に於いて、該リン化硼素半導体層の下層部が、硼素(B)とリン(P)とを含む非晶質からなり、該リン化硼素半導体層の上層部が、表面を{111}-結晶面とするリン化硼素単結晶({111}-リン化硼素単結晶)であって、平面形状を略正三角形とする複数の板状結晶を連結させた単結晶層からなることを特徴とするリン化硼素系半導体素子。

【請求項2】

前記板状結晶の各々の三角形が、ひとつの頂点を同一方向に向けて配置されていることを特徴とする請求項1に記載のリン化硼素系半導体素子。 10

【請求項3】

前記板状結晶の各々の三角形の一辺が、珪素単結晶基板の<110>方向に略平行または略垂直であることを特徴とする請求項1または2に記載のリン化硼素系半導体素子。

【請求項4】

表面を{111}-結晶面とする珪素(Si)単結晶からなる基板上に、下層部と上層部とからなるリン化硼素(BP)半導体層を形成するリン化硼素系半導体素子の製造方法に於いて、硼素源と、硼素源の濃度に対して第1の濃度比率(R_1)のリン源とを供給して非晶質の下層部を形成する第1の工程と、その後、硼素源に対するリン源の濃度比率を R_1 より大きな第2の濃度比率(R_2)に経時的に増加させて、表面を{111}-結晶面とするリン化硼素単結晶({111}-リン化硼素単結晶)であって、平面形状を略正三角形とする複数の板状結晶を連結させた単結晶層からなる上層部を下層部上に形成する第2の工程とにより、リン化硼素半導体層を形成することを特徴とするリン化硼素系半導体素子の製造方法。 20

【請求項5】

R_1 を0.2以上50以下とし、 R_2 を500以上2000以下とすることを特徴とする請求項4に記載のリン化硼素系半導体素子の製造方法。

【請求項6】

請求項1乃至3のいずれか1項に記載のリン化硼素系半導体素子であって、リン化硼素半導体層の上に窒化ガリウム・インジウム混晶($Ga_xIn_{1-x}N$)層からなる発光層を設けて作製したLED。 30

【発明の詳細な説明】

【0001】

【発明の属する技術分野】

本発明は、珪素(Si)単結晶基板の表面上に形成されたリン化硼素半導体層を具備するリン化硼素系半導体素子とその製造方法に係わり、特に表面の平坦性に優れ、結晶欠陥が少ないリン化硼素半導体層を具備するリン化硼素系半導体素子に関する。

【0002】

【従来の技術】

従来より、リン化硼素(BP)半導体層は、種々の半導体素子を構成するために利用されている。例えば、npn接合型ヘテロバイポーラトランジスタ(HBT)のn形ベース(base)層を構成するに利用されている(J. Electrochem. Soc., 125(4)(1978)、633~637頁参照)。また、青色のレーザダイオード(LED)にあって、接触抵抗の低いオーミック(Ohmic)電極を形成するためのコンタクト(contact)層として利用されている(特開平10-242567号公報参照)。また、青色光等の短波長の発光をもたらす発光ダイオード(LED)を構成するための緩衝層として用いられている(米国特許6,069,021号参照)。

【0003】

リン化硼素半導体層は、従来から三塩化硼素(BCl_3)や三塩化リン(PCl_3)を出発原料とするハロゲン(halogen)法(『日本結晶成長学会誌』、Vol. 24、 50

No. 2 (1997)、150頁参照)、ボラン(BH_3)またはジボラン(B_2H_6)とホスフィン(PH_3)等を原料とするハイドライド(hydride)法(J. Crystal Growth, 24/25 (1974)、193~196頁参照)、分子線エビタキシャル法(J. Solid State Chem., 133 (1997)、269~272頁参照)、及び有機硼素化合物とリンの水素化合物を原料とする有機金属化学的気相堆積(MOCVD)法(Inst. Phys. Conf. Ser., No. 129 (IOP Publishing Ltd. (UK, 1993)、157~162頁参照)等により形成されている。

【0004】

リン化硼素半導体層を気相成長させたための基板には、もっぱら、珪素単結晶(シリコン)が使用されている(上記の▲1▼J. Electrochem. Soc., 125 (1978)参照)。しかし、珪素単結晶の格子定数は 5.431Å であり、立方晶閃亜鉛鉱型のリン化硼素の格子定数は 4.538Å である(寺本 巖著、「半導体デバイス概論」(1995年3月30日、(株)培風館発行初版)、28頁参照)。従って、珪素単結晶とリン化硼素結晶との格子ミスマッチ度は約16.5%と大きくなっている(庄野 克房著、「半導体技術(上)」(1992年6月25日、(財)東京大学出版会発行9刷)、97~98頁参照)。

10

【0005】

また、珪素単結晶基板上で単結晶のリン化硼素半導体層が成長するのは、例えばハロゲン気相成長法では、 1020°C から 1070°C の 50°C の極めて狭い温度の範囲に限定されるのが知れている(西永 頌、「応用物理」(第45巻第9号(1976)、891~897頁参照)。また、ボラン(BH_3)とホスフィン(PH_3)を原料とするハイドライド法では、気相成長条件の僅かな変化に因り、リン化硼素半導体層内に一種の積層欠陥(stacking fault)である双晶(twinning)が発生してしまうのが教示されている(上記の「半導体技術(上)」、99~100頁参照)。

20

【0006】

【発明が解決しようとする課題】

珪素基板表面上にリン化硼素半導体層を気相成長手段させるに際しての従来技術の問題点は、リン化硼素半導体層と珪素単結晶との格子ミスマッチが大であり、それを十分に緩和させるに有効な結晶構成或いは製造方法が明確となっていないために、表面の平坦性に優れるリン化硼素半導体層を定常的に得られないことにあった。さらに、単結晶のリン化硼素半導体層を気相成長できる温度の範囲が狭く、またわずかな気相成長条件の変化に因って双晶が発生するなどの理由により、結晶欠陥の少ないリン化硼素の単結晶層をそもそも安定して製造できなかった。従って、良好な特性を発揮できるリン化硼素系半導体素子を十分に安定して提供するに至らなかった。

30

【0007】

本発明は、表面の平坦性に優れ結晶欠陥が少ないリン化硼素半導体層を具備し、良好な特性を発揮できるリン化硼素系半導体素子とその製造方法を提供することを目的とする。

【0008】

【課題を解決するための手段】

即ち本発明は、

40

(1) 表面を $\{111\}$ -結晶面とする珪素(Si)単結晶からなる基板と、該基板表面上に設けられたリン化硼素(BP)半導体層とを備えたリン化硼素系半導体素子に於いて、該リン化硼素半導体層の下層部が、硼素(B)とリン(P)とを含む非晶質からなり、該リン化硼素半導体層の上層部が、表面を $\{111\}$ -結晶面とするリン化硼素単結晶($\{111\}$ -リン化硼素単結晶)であって、平面形状を略正三角形とする複数の板状結晶を連結させた単結晶層からなることを特徴とするリン化硼素系半導体素子。

(2) 前記板状結晶の各々の三角形が、ひとつの頂点を同一方向に向けて配置されていることを特徴とする上記(1)に記載のリン化硼素系半導体素子。

(3) 前記板状結晶の各々の三角形の一辺が、珪素単結晶基板の $\langle 110 \rangle$ 方向に略平行

50

または略垂直であることを特徴とする上記(1)または(2)に記載のリン化硼素系半導体素子。

(4) 表面を{111}-結晶面とする珪素(Si)単結晶からなる基板上に、下層部と上層部とからなるリン化硼素(BP)半導体層を形成するリン化硼素系半導体素子の製造方法に於いて、硼素源と、硼素源の濃度に対して第1の濃度比率(R_1)のリン源とを供給して非晶質の下層部を形成する第1の工程と、その後、硼素源に対するリン源の濃度比率を R_1 より大きな第2の濃度比率(R_2)に経時的に増加させて、表面を{111}-結晶面とするリン化硼素単結晶({111}-リン化硼素単結晶)であって、平面形状を略正三角形とする複数の板状結晶を連結させた単結晶層からなる上層部を下層部上に形成する第2の工程とにより、リン化硼素半導体層を形成することを特徴とするリン化硼素系半導体素子の製造方法。

10

(5) R_1 を0.2以上50以下とし、 R_2 を500以上2000以下とすることを特徴とする上記(4)に記載のリン化硼素系半導体素子の製造方法。

(6) 上記(1)乃至(3)のいずれか1項に記載のリン化硼素系半導体素子であって、リン化硼素半導体層の上に窒化ガリウム・インジウム混晶($Ga_xIn_{1-x}N$)層からなる発光層を設けて作製したLED。

である。

【0009】

【発明の実施の形態】

本発明に係わるリン化硼素半導体層は、ハロゲン法、ハイドライド法、分子線エピタキシャル法、及びMOCVD法等の気相成長手段に依り、表面を{111}-結晶面とする珪素単結晶({111}-珪素単結晶)の表面上に成長させる。{111}-珪素単結晶の表面をなす{111}-結晶面には、他の低次のミラー(Miller)指数面に比較してSi原子が密に存在しているため、硼素及びリンの珪素単結晶基板内部への浸透、拡散を抑制するに優位となる。気相成長を実施する温度としては、750℃~1200℃が適する。1200℃を超える高温は、 $B_{13}P_2$ 等の多量体のリン化硼素結晶(J. Am. Ceramic Soc., 47(1)(1964)、44~46頁参照)が発生するため、単量体の単結晶のリン化硼素層を形成するに不都合となる。リン化硼素半導体層の成長を妨害する酸化珪素膜を表面に形成させないために、珪素単結晶基板は酸素雰囲気内ではなく、非酸化性の雰囲気中で加熱するのが好適である。また、リン化硼素半導体層の気相成長を妨害(マスキング)する窒化珪素膜の形成を避けるために窒素(N_2)を含まない雰囲気中で加熱するのが適する。水素雰囲気或いはアルゴン(Ar)等の単原子不活性ガスからなる雰囲気は好適に利用できる。

20

30

【0010】

本発明のリン化硼素半導体層は、内部の結晶構成に特徴があり、下層部は硼素とリンとを含む非晶質から構成されるものとなっている。下層部とは、リン化硼素半導体層の表面に対して下方の底部に位置する層である。硼素とリンとを含む非晶質層は、気相成長時に於ける硼素源の濃度に対するリン源の濃度の比率、所謂、V/I/I比率を比較的に低値とすることにより形成できる。特に、V/I/I比率を0.2以上で50以下に設定することで効率的に形成できる。なお、硼素源およびリン源の濃度は、それぞれモル濃度で表わすものとする。0.2未満の極端に低いV/I/I比率では、硼素の濃度が相対的に過剰となり、半球状の硼素の結晶粒が密集した表面の平坦性に欠ける非晶層を帰結する不都合を生ずる。50を超えるV/I/I比率では、非晶質層内に単結晶粒が散在する多結晶のリン化硼素層が形成される場合があり、確実に非晶質を形成できず好ましくはない。非晶質または多結晶、単結晶の判別は、X線回折手段または電子線回折法に依り判別できる。

40

【0011】

V/I/I比率を上記の第1のV/I/I比率(R_1 とする)として気相成長させた非晶質層上には、リン化硼素半導体層の上層部として、第2のV/I/I比率(R_2 とする)をもってリン化硼素の単結晶層を形成する。本発明のリン化硼素半導体層の上層部は、図1に模式的に例示する如く、表面を{111}-結晶面とするリン化硼素単結晶({111}

50

1}ーリン化硼素単結晶)であって、略正三角形の平面形状を有する複数の板状結晶10が積重した単結晶層からなる。ここで板状結晶10の一辺の長さはおよそ100~200nmである。また、板状結晶10は三角形の底辺11に対し、頂点12が同一の方向に配置されているのが特徴である。同一の方向に画一的に板状結晶10を配置することにより、鏡像関係の位置に配置した、所謂、二重配置(double spacing)の結晶体(橋口 隆吉、近角 聡信編著、「薄膜表面現象」(朝倉書店発行材料科学講座6)、49~50頁参照)に起因する双晶の発生が防止でき、結晶欠陥の少ないリン化硼素単結晶層を得るに効果を上げられる。略正三角形の板状単結晶体が配置されている方向は、例えば原子間力顕微鏡(AFM)を利用したリン化硼素単結晶層の表面の観察に依り判定できる。

10

【0012】

特に、略正三角形の板状結晶10を、一辺13を珪素単結晶の<110>結晶方向に略平行となる様に配置させると、ダイヤモンド(diamond)結晶構造の珪素単結晶の劈開方向が<110>結晶方向であることと相俟って、リン化硼素単結晶層を劈開により簡単に分割するに利便となる。一辺13を珪素単結晶基板の<110>結晶方向に略平行或いは垂直とし、且つ、同一の方向に画一的に配置したリン化硼素の板状結晶を気相成長させるには、第2の比率(=R₂)を500以上で2000以下とする必要がある。板状結晶を気相成長させる温度を高温とする程、R₂を高値とするのが好ましい。第1の比率(=R₁)と同じく第2の比率(=R₂)は、気相成長時に於ける硼素源及びリン源の供給量を例えば質量流量計(MFC)等に依り、精密に制御して調整する。板状のリン化硼素単結晶体の厚さは、硼素源の供給時間を調整すれば制御できる。

20

【0013】

第2の比率(=R₂)が500未満であると、頂点部に丸みを帯びた略正三角形の板状のリン化硼素単結晶体が得られ、また、多くはこれらの板状結晶と非晶質とが混在する層が得られる。また、R₂が2000を超えると、珪素単結晶基板の{110}結晶方向に略平行或いは垂直な一辺を有する略正三角形の板状のリン化硼素単結晶体を安定して得るにいたらない。R₂を大とする程、珪素単結晶の{110}結晶方向と略正三角形の板状単結晶体の一辺とがなす角度は大となる傾向にある。R₂を上記の好適な比率に設定するに加え、R₁の比率をもって気相成長させる非晶質層の層厚を薄くすると、画一的な方向に配置し、且つ一辺を珪素単結晶基板の{110}結晶方向に略平行或いは垂直とする略正三角形の板状リン化硼素単結晶体を得ることができる。非晶質層の層厚は、好ましくは2nm以上で20nm以下とする。非晶質の層厚が増加すると共に、珪素単結晶の{111}一結晶面の影響力は弱まり、平面形状を略三角形とする板状のリン化硼素単結晶体すら定常的に得られなくなる。

30

【0014】

R₁よりR₂へとV/I/I比率を増加させるには、例えば、硼素源の気相成長系への供給量を一定に保持しつつ、リン源の供給量を経時的に段階的に増量させれば、V/I/I比率を増加できる。例えば、(C₂H₅)₃Bの供給量を一定としつつ、PH₃の流量を段階的に増加させてV/I/I比率を増加させる。または、リン源の供給量を一定に維持しつつ、硼素源の供給量を減少させて、V/I/I比率をR₂に増加させる。或いは、硼素源の供給量の増加率を上回る増加率でリン源の供給量を増加させてV/I/I比率を増加させる。硼素源は、略正三角形の板状のリン化硼素単結晶体の成長速度(層厚の増加速度)が毎分15nmから毎分30nmとなる様に供給するのが好適である。成長速度を極端に減少させることは、成長時間の延長を招く。即ち、珪素単結晶基板及び硼素とリンとを含む非晶質層とが高温で暴露される時間を延長させ、硼素またはリンとSi結晶との反応を促進させ、珪素単結晶基板と非晶質層との接合界面を乱雑化させる不都合を招く。

40

【0015】

上層部のリン化硼素単結晶層は、上記の如く一定の方向を持って配置した略正三角形の板状の{111}ーリン化硼素単結晶体から構成されている。従って、含まれる双晶(または積層欠陥)の少ない良質のリン化硼素単結晶となっている。また、各板状単結晶体の

50

表面は、 $\{111\}$ —珪素単結晶基板の表面をなす $\{111\}$ —珪素結晶面に平行に配列したリン化硼素の $\{111\}$ —結晶面から画一的に構成されているため、平坦となっている。従って、本発明に係わるリン化硼素単結晶層上には、伝搬して来る双晶も少なく、表面の平坦性に優れる上層を形成できる。例えば、結晶欠陥密度の小さな良好な結晶性の窒化ガリウム(GaN)系半導体層を上層として形成できる。リン化硼素系半導体素子、例えばLEDは、上記の結晶性に優れるGaN層を下部クラッド層として備えた積層構造体にオーミック(Ohmic)性の入・出力電極を設けて構成する。

【0016】

【作用】

第1の V/III 比率 R_1 をもって形成した硼素とリンとを含む非晶質上に気相成長させた、平面形状を略正三角形とし、同一の方向に画一的に配列した $\{111\}$ —リン化硼素単結晶からなる平板状の単結晶体は、双晶(または積層欠陥)密度が小さい良質の単結晶層を含むリン化硼素半導体層をもたらす作用を有する。また、特に劈開方向である珪素単結晶基板の $\langle 110 \rangle$ 結晶方向に略平行或いは略垂直な方向に、略正三角形の一辺を配列した $\{111\}$ —リン化硼素単結晶からなる板状の単結晶体は、リン化硼素半導体層の $\langle 110 \rangle$ 結晶方向への劈開を容易とする作用を有する。

【0017】

【実施例】

(第1実施例)

本第1実施例では、 $\{111\}$ —珪素単結晶基板上に、常圧MOCVD手段に依りリン化硼素(BP)半導体層を気相成長させた場合を例にして、本発明の内容を具体的に説明する。

【0018】

本第1実施例では、 $[110]$ 結晶方向に角度にして 2° 傾斜した $\{111\}$ —珪素結晶面を表面とする珪素単結晶を基板として利用した。基板を高純度グラフアイト製の載置台(susceptor)上に水平に載置した後、高純度の石英角筒製MOCVD気相成長炉内の気相成長領域に挿入した。その後、気相成長炉内に毎分約16リットルの高純度水素ガスをキャリア(carrier)ガスとして流通しつつ、高周波誘導加熱方式により、基板の温度を 850°C に昇温した。然る後、硼素源としたトリエチル硼素(C_2H_5)₃B)及びリン源としたホスフィン(PH_3)を気相成長領域に供給した。トリエチル硼素は、水素ガスで発泡させ、その発泡用水素ガスに、トリエチル硼素の蒸気を随伴させることにより供給した。発泡用水素ガスの流量は、電子式質量流量計(MFC)を使用して毎分45ccに精密に制御した。随伴されるトリエチル硼素の濃度は、標準状態(0°C 、1気圧)に於いて、毎分 1.34×10^{-4} モル(mol)と換算された。一方、気相成長領域に供給されるホスフィンの濃度は、 2.14×10^{-3} モル/分とした。即ち、 V/III 比率は16.0となった。硼素源及びリン源を上記の濃度で供給しつつ、且つ V/III 比率を上記の第1の比率(R_1 、但し $R_1=16$)に維持しつつ、2.5分間に亘り硼素源及びリン源の気相成長領域への流通を継続した。これより、層厚を20nmとする硼素とリンとを含む非晶質層を $\{111\}$ —Si基板上に形成した。

【0019】

上記の非晶質層の気相成長を終了させると同時に、気相成長領域へ供給する硼素源の濃度を 1.49×10^{-5} モル/分に減じ、併せて、リン源の供給量を 1.93×10^{-2} モル/分へ増加させた。即ち、 V/III 比率を第1の V/III 比率(R_1)より第2の V/III 比率(R_2)の1295.3に上昇させた。第2の V/III 比率をこの値に維持しつつ、硼素源及びリン源の供給を5分間に亘り継続して、上記の非晶質層上に層厚を300nmとするp形のリン化硼素半導体層を形成した。硼素源の気相成長領域への供給を停止してリン化硼素半導体層の形成を終了した後は、水素キャリアガスとホスフィンとからなる混合気体雰囲気内で $\{111\}$ —珪素単結晶基板を室温近傍の温度迄、強制的ではなく自然に冷却した。

【0020】

冷却後、上記の非晶層の結晶形態を一般のX線回折測定並びに電子線回折測定に依り確認した。X線回折測定並びに電子線回折測定とも、回折斑点の無いハロー(halo)な回折パターンが得られ、非晶質層であると認められた。一方、リン化硼素半導体層のX線回折パターンには、リン化硼素の(111)-結晶面からの回折が出現した。リン化硼素半導体層の(111)-結晶面からの明瞭な回折ピークの出現は、非晶質層を本第1実施例の如く、適度な薄層としたため、基板の表面をなす(111)-Si結晶面の配列を受け継いだためと解釈された。また、一般の原子間力顕微鏡(AFM)を使用してリン化硼素半導体層の表面を観察したところ、表面の全面に(111)-リン化硼素結晶の平面形状を反映して、図1に例示した如くの略正三角形の複数の板状結晶が積重しているのが視認された。略正三角形の板状結晶は、基板の珪素単結晶の<110>方向に平行な画一的な向きに整列していた。

10

【0021】

(第2実施例)

本第2実施例では、本発明に係わるリン化硼素半導体層を備えた積層構造体を使用してLEDを作製する場合を例にして、本発明の内容を具体的に説明する。

【0022】

図2に本第2実施例に係るLED1Aの平面模式図を示す。また、図3には、図2に示す破線X-X'に沿ったLED1Aの断面模式図を示す。

【0023】

上記の第1実施例と同様の方法により、p形の(111)-珪素単結晶基板101上に、V/III比率を $R_1 (=16.0)$ として硼素とリンとを含む非晶質層102を気相成長させ、さらにV/III比率を $R_2 (=1295.3)$ としてp形リン化硼素半導体層103を気相成長させた。本第2実施例に係るLEDでは、単量体の(111)-リン化硼素単結晶からなるp形リン化硼素半導体層103を下部クラッド層103として利用した。下部クラッド層103をなす(111)-p形リン化硼素半導体層のキャリア濃度は約 $2 \times 10^{19} \text{ cm}^{-3}$ であった。

20

【0024】

下部クラッド層103上には、発光層104及びn形リン化硼素層からなる上部クラッド層105を順次積層させてLED1A用途の積層構造体1Bを形成した。発光層104はn形の窒化ガリウム・インジウム混晶($\text{Ga}_x\text{In}_{1-x}\text{N}$)層から構成した。 $\text{Ga}_x\text{In}_{1-x}\text{N}$ 層は、トリメチルガリウム($(\text{CH}_3)_3\text{Ga}$)、トリメチルインジウム($(\text{CH}_3)_3\text{In}$)、アンモニア(NH_3)、窒素(N_2)反応系のMOCVD法を利用して 850°C で形成した。六方晶ウルツ鉱結晶型の $\text{Ga}_x\text{In}_{1-x}\text{N}$ のインジウム組成比($=1-x$)は、p形リン化硼素半導体層103の表面をなすリン化硼素の(111)-結晶面に鉛直に交差するリン化硼素の{110}-結晶面の間隔(約 3.21\AA)に合致するa軸の格子定数となるように10%($=0.10$)とした。次に、トリエチル硼素の蒸気を随伴する発泡用水素ガス及びホスフィンの気相成長領域への添加を再開して、上部クラッド層105をなすn形のリン化硼素結晶層を形成した。n形リン化硼素結晶層105の層厚は約 300 nm とした。また、通常の電解C-V法に依り測定された同層105のキャリア濃度は約 $1 \times 10^{19} \text{ cm}^{-3}$ であった。トリエチル硼素の蒸気を随伴する発泡用水素ガスの気相成長領域への添加を停止して、n形リン化硼素結晶層105の形成を終了した。その後、リン源(PH_3)と水素キャリアガスとの混合雰囲気中で積層構造体1Aの温度を約 600°C に降温した。その後、気相成長領域への PH_3 の供給を停止し、 H_2 気流中で積層構造体1Aを室温近傍迄、冷却した。

30

40

【0025】

積層構造体1Bの表層をなすn形リン化硼素結晶層からなる上部クラッド層105の中央部には、同層105に接触する側に金・ゲルマニウム($\text{Au} \cdot \text{Ge}$)合金膜を配置したAu・Ge-ニッケル(Ni)-Auの3層重層構造からなるn形オーミック電極107を設けた。結線用の台座(pad)電極を兼ねるn形オーミック電極107は、直径を約 $150\text{ }\mu\text{m}$ とする円形の電極とした。また、p形珪素単結晶基板101の裏面の略全面には

50

、金（Au）からなるp形オーミック電極108を配置した。Au蒸着膜の膜厚は約3 μ mとした。これより、n形発光層104をp形リン化硼素層103及びn形リン化硼素層105で挟持したpn接合型DH構造のLED1Aを構成した。p形リン化硼素層103及びn形リン化硼素層105は、何れも室温で約3eVの禁止帯幅を有するため、発光層104に対する障壁層（clad）層として有効に利用できた。

【0026】

積層構造体1Bを珪素単結晶基板101の<110>結晶方向に劈開して、一辺を約350 μ mとする正方形のチップ（chip）に分割した。下部クラッド層103の（111）-リン化硼素半導体層をなす（111）-板状結晶は、一辺を<110>方向に平行または垂直な方向に画一的に配置しているため、<110>結晶方向への劈開は容易に実施できた。n形オーミック電極107とp形オーミック電極108との間に順方向に20ミリアンペア（mA）の動作電流を通流したところ、LED1Aから波長を約440nmとする青紫帯光が発せられた。一般的な積分球を利用して測定されるチップ状態での輝度は9ミリカンデラ（mcd）となり、高発光強度のLED1Aが提供されることとなった。また、硼素とリンとを含む非晶質層102を介して設けたp形リン化硼素半導体層103の表面は平坦性に優れるものであったため、n形発光層104とで接合界面を平坦とするpn接合構造を形成できた。また、表面の平坦なp形リン化硼素半導体層103を下地層としたため、発光層104の表面も好都合に平坦となり、上部クラッド層105とで平坦な接合界面のpn接合構造を形成できた。このため、順方向電圧（但し、順方向電流を20mAとした場合）を約3.1Vとし、逆方向電圧（但し、逆方向電流を10 μ Aとした場合）を5V以上とする良好なpn接合構造に基づく整流特性を有するリン化硼素系LEDが提供されることとなった。

【0027】

【発明の効果】

表面を{111}-結晶面とする珪素単結晶からなる基板と、基板表面の{111}-結晶面上に設けられたリン化硼素半導体層を備えてなるリン化硼素系半導体素子に於いて、本発明に依れば、該リン化硼素半導体層の下層部が、硼素（B）とリン（P）とを含む非晶質からなり、該リン化硼素半導体層の上層部が、表面を{111}-結晶面とするリン化硼素単結晶（{111}-リン化硼素単結晶）であって、平面形状を略正三角形とする複数の板状結晶を連結させた単結晶層からなるように構成したので、表面の平坦性に優れるリン化硼素単結晶層を従来に無く広い温度範囲に於いて気相成長できる。従って平坦な接合界面を有するpn接合構造を構成でき、しいては、良好な整流特性をもったリン化硼素系半導体発光素子をもたらすに貢献できる。

【0028】

本発明ではまた、リン化硼素半導体層をなす上層部の板状結晶の各々の三角形が、ひとつの頂点を同一方向に向けて配置されているようにしたので、双晶等の結晶欠陥密度の小さな結晶性に優れるリン化硼素単結晶層を安定して気相成長するに効果を上げられ、しいては、良好なpn接合特性を発揮できるリン化硼素系半導体素子をもたらすに貢献できる。

【0029】

また本発明では、リン化硼素半導体層の上層部をなす板状結晶の各々の三角形の一辺が、珪素単結晶基板の<110>方向に略平行または略垂直であるよう、画一的な方向に整列させて配置することとしたので、珪素単結晶の<110>方向への劈開を利用して、簡易に個別のリン化硼素系半導体素子が得られる。

【0030】

また、本発明に依れば、気相成長時に供給する硼素源とリン源の濃度比率を0.2以上で50以下として非晶質の下層部を形成した後、硼素源とリン源の濃度比率をより大きな500以上で2000以下とし、略正三角形の{111}-リン化硼素単結晶からなる板状結晶を非晶質上に気相成長させることにより、上層部をなすリン化硼素単結晶層を形成することとしたので、双晶等の結晶欠陥密度が小さく、表面の平坦性に優れ、劈開に依る個別の素子への分離を容易にするリン化硼素単結晶層をもたらすに効果が奏される。

【図面の簡単な説明】

【図 1】 平面形状を略正三角形とする複数の板状結晶を連結させた単結晶層からなるリン化硼素半導体層の上層部を示す模式図である。

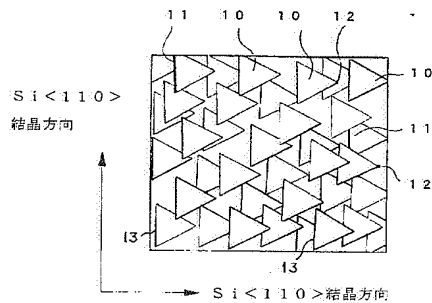
【図 2】 本発明の第 1 実施例に係る L E D の平面模式図である。

【図 3】 図 2 に示す L E D の破線 X - X' に沿った断面模式図である。

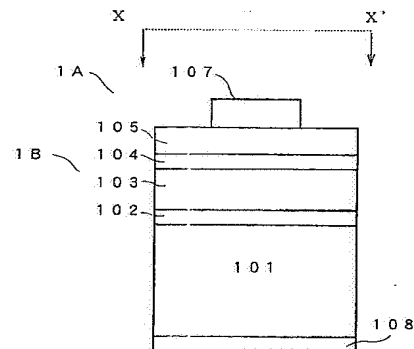
【符号の説明】

- 1 0 平面形状を略正三角形とするリン化硼素単結晶からなる板状結晶
- 1 1 板状結晶の底辺
- 1 2 板状結晶の一頂点
- 1 3 板状結晶の一辺
- 1 A L E D
- 1 B 積層構造体
- 1 0 1 単結晶基板
- 1 0 2 非晶質層
- 1 0 3 リン化硼素単結晶層（下部クラッド層）
- 1 0 4 発光層
- 1 0 5 上部クラッド層
- 1 0 7 n 形オーミック電極
- 1 0 8 p 形オーミック電極

【図 1】



【図 3】



【図 2】

